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PRIMARY RESEARCH

Design and simulation of optimized QPSK transmitter using HDL code in MATALB

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Abstract
In this paper, the design and simulation of the QPSK transmitter using HDL code in MATLAB are presented. Different applications in DSP require mathematical modeling for investigation and analysis due to the complexity of HDL code language. The idea of design the HDL-SIMULINK form using MATLAB is to offer enough facility to modify and improve the wireless communication systems. Implementing any DSP model in real time based on FPGA platforms requires translating the MATLAB-SIMULINK model to HDL code before the bit generation is downloaded to this board. The floating-point implementation should be transferred to a fixed point for a high dynamic range of applications. An alternative approach has been proposed based on HDL code, and the property of simulation environments in MATLAB is designed. The data transfer, synchronization, and driving sample between Simulink and HDL language are explained in this paper.

I. INTRODUCTION

Nowadays, the most challenge faced the researcher in wireless communication systems is to bring high features devices to the marketplace rapidly with high reliability and flexibility [1, 2, 3]. The alterations and developments have to be probable with no complexity to control the current design such as elevated height synthesis and planning robotically [4, 5, 6]. Due to these problems of proper formulation in the system design, the concept part is extremely critical [2, 7]. Several years ago, the HDL was developed and introduced by many researchers in this field [4, 5]. The automated tools and HDL language have been produced new abilities to the researchers with some limitations which required overcoming early [8, 9, 10]. In this area, the researcher looks for new tools to deal with model and explanation of high level abstraction design and implementations. Since some years ago, the terms of co-design, co-simulation and system level design have well known with incoming SDR technology [11, 4, 12]. The strong impact on the model is the system complexity that is expected to reflect the functionality of the system with timing concentrations [5, 13]. The HDL language such as Verilog or VHDL is intended for many reasons. Therefore, to describe each algorithm in the tools have to describe as well which required high skills is [14, 15]. In software design, the high level system in DSP design is automatically converted to the RTL and the results could be synthesized to Xilinx product such as FPGAs by uesing the ISE software tools [15, 16]. Then, the entire bit stream can down load to FPGA in succeeded steps include place & route and synthesis process which automatically performs the FPGA files [17, 18]. These comparative steps of software are equivalent to inherent massive parallelism of FPGA which allow implementing the abstraction design by so called co-simulation adoptions [19, 20]. The SIMULINK block set in MATLAB programs is an environments used for different area to design a active and entrenched systems [21, 22]. The system generator represent high level tool could be used to facilitate the FPGA kits design [23, 24]. This paper is produced new design approach to modeling a complex mathematical design using HDL platforms of wireless communication transmitter. The high level technical computing language in MATLAB is used as data visualization and analysis to optimize the HDL code using system generator and MATLAB as show in Figure 1.

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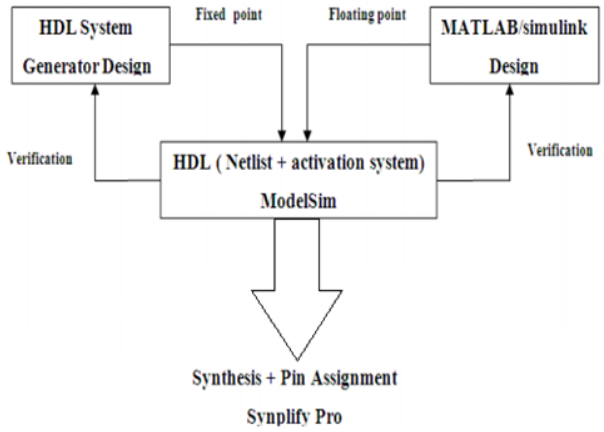

Fig. 1. Optimized HDL code design flow

The Xilinx ISE require synthesis files in Electronic Design Interface File (EDIF) and User Constraint File (USF) to optimize the integrated design of HDL-QPSK transmitter model. The NCD file is converting first to configuration bit stream which is downloading to FPGA via JTAG program file. The results of translate; map, place and route should indicate no error before performing the bits download to FPGA. Figure 2 illustrate the flow chat of optimizing the HDL code for QPSK transmit part.

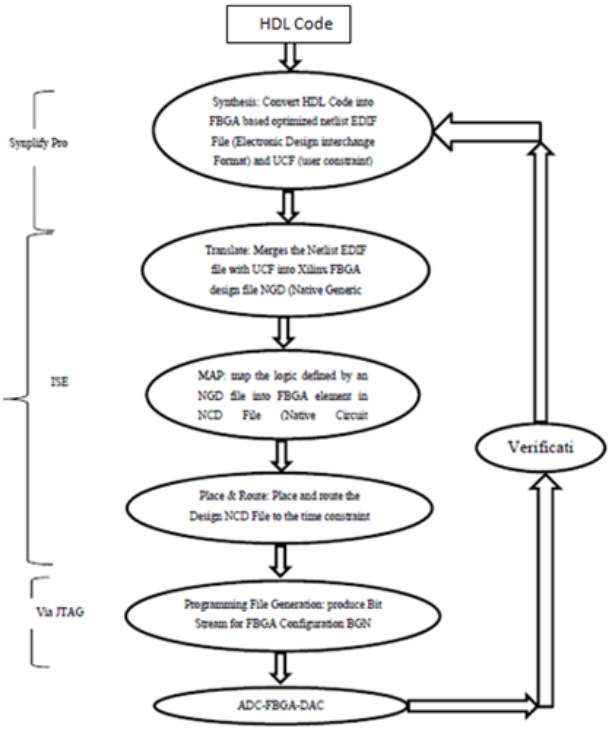

Fig. 2. Optimize HDL synthesis flow diagrams

II. OPTIMIZATION OF HDL CODE OF QPSK TRANSMITTER

The optimization of HDL code of QPSK transmitter model shown in Figure 3 has been designed and modeled in MATLAB-SIMULINK block set to support the code generation for baseband processing of digital communication systems. In the high level chain, the HDL transmitter generates a complex valued after modulated by QPSK scheme, symbol mapping and pulse shaping by matching RRC filter. The pipeline register is put in among the systems to reduce the delay and exploit the frequency of data clock.

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Hence, the fixed latency is achieved before valid information is appearing at the RRC filter input. Valid out and valid in are include controlling the multiplexer and ensuring the valid data is transmitted.

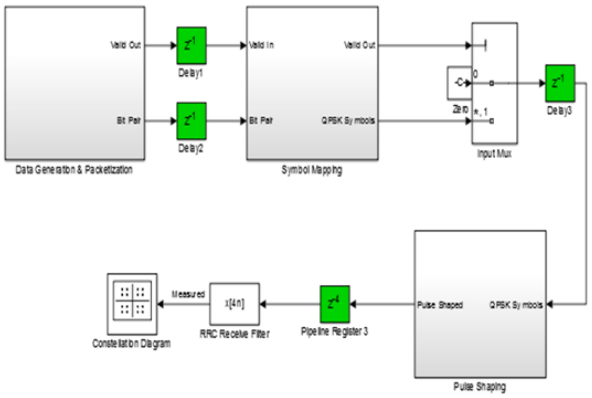

Fig. 3. Optimized HDL of QPSK transmitter model

The information source is used to generate the introduction and data bits with picketing and scrambling process. Figure 4 illustrate the full structure of source generator block components. The generated data packets contain 26 bit barker type code as introduction data and 174 bits as scrambler part. To convert the data input from serial forms into two bits output with 1/2 sampling speed, a bit pairing block is used to provide correct data format in sampler mapping part. This data is delayed by two samples via pipeline delay to control the down sample signal which is reducing the sample rate by two. The FSM components contain more machine to produce by charting capability of state flow with three state named 1, 2 and append data.

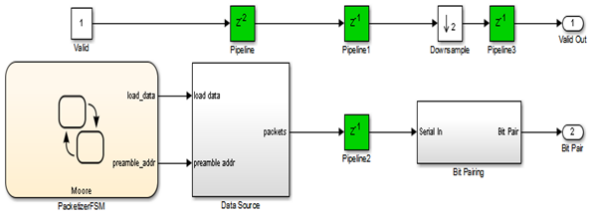

Fig. 4. Data source generator subsystems

The 1 and two states are used to serve the increment adder output from zero to 25. Hence, state zero included as unitization state to address from zero and state 1 increment to address counter from remaining clock period. After that, the FSM will change to join the data to emphases the signal of used data signal if it remains for 147 cycles or not. In sequence, the FSM shall switch between the above three states through the running. The data source showing in Figure 5 contain two look up tables one for data bit and the other for introduction data bits.

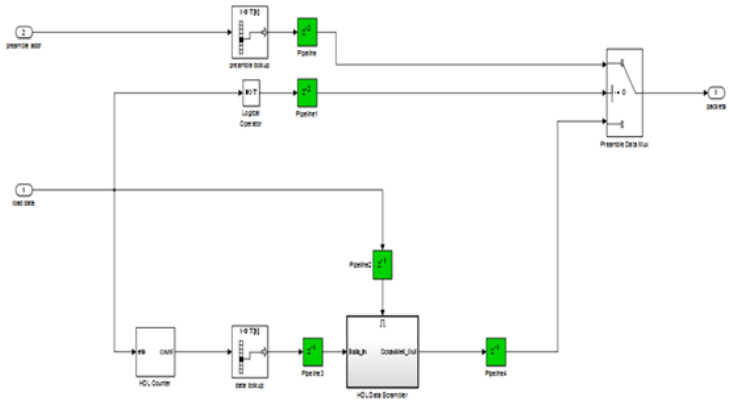

Fig. 5. data source structure

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The introduction LUT is addressed by packet FSM through the adder and the LUT of data is addressed by counter to enable the FSM for correct number of clock cycles to remains constant for every packets. On the other hand, the data LUT address sequence is vary of different data bits consist in inside every packet and all LUT is insertion of zero to make sure that the number of information entry is a authority of two lengths. In order to enable the counter of LUT data, the input data loaded is used to organize the data of scrambler section and if the data bits are passing into the output through the MUX. The data scrambler is design by use XOR gates and register which is enabling only when the input data is processed. Figure 6 illustrate the structure of data scrambler in the system. The bit pairing subsystems is used to grouping the pairs of bits into the output bits which is an expected input to symbol mapping blocks. This process is done by using a pair of the down sampler to decrease the sample speed by two. Thus, the first down sampler selects another phase and second down sampler select the first phase as illustrated in Figure 7.

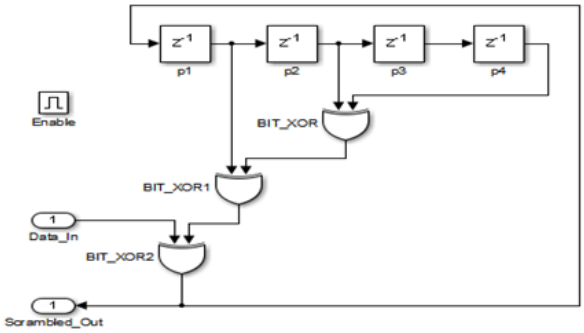

Fig. 6. Data scrambler design

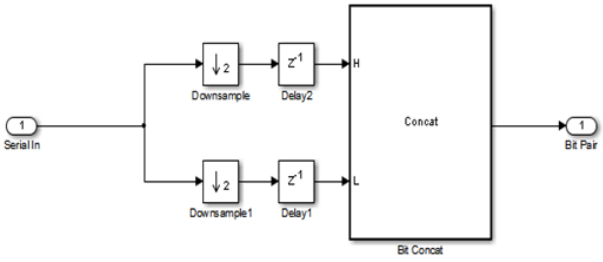

Fig. 7. Bit pairing subsystems

The QPSK modulator have use a symbol mapping from communication block sets to perform the map integer value from 0,1,2,3 into correct complex values symbol as shown in Figure 8.

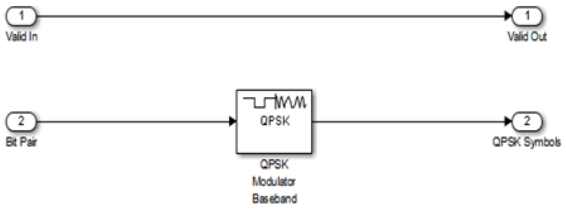

Fig. 8. Symbol mapping system

The pulse shaping section in proposed model consist of an FIR interpolation filter to perform up-sampling factor by 4 with RRC impulse response behavior to match the receive filter response in the receiver section. The pipeline of this filter is to ensure the combination delay which produce high throughput in the design. The subsystem model of interpolation filters with the input and output port is illustrated in Figure 9.

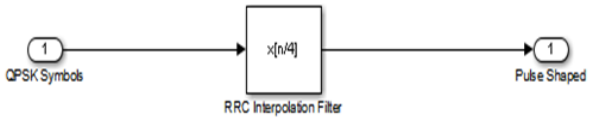

Fig. 9. Pulse shaping interpolation filter model

III. RESULTS ANALYSIS

After the model was running, the constellation and eye diagrams of the passing signal through the transmitter and receiver filter is obtained as illustrate in Figure 10 and Figure 11. In same time, the difference between the value of error vector in ideal constellation points and the constellation points produced after transmit and receiver filtering is carried out as well.

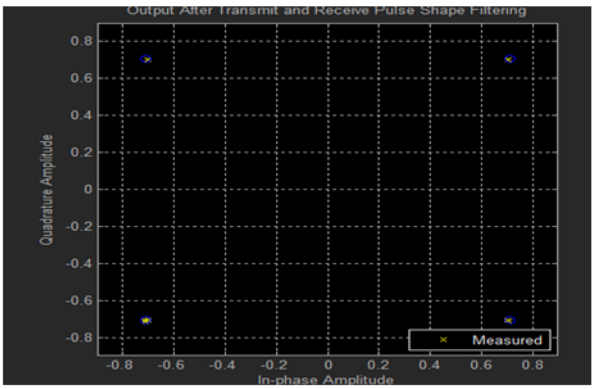

Fig. 10. Constellation points of transmit and receive signals

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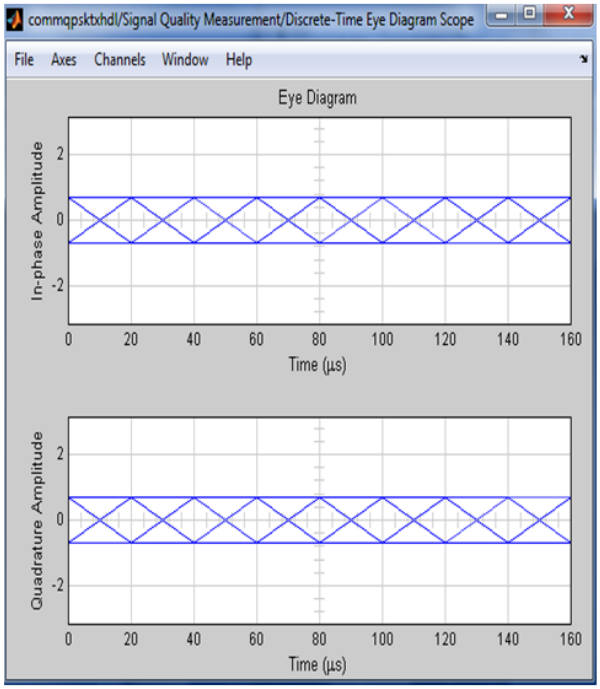

Fig. 11. Eye diagram of QPSK transmitted signal

The figure produced by EVM represent the merit regarding to the distortion caused by transmitting and received filters which allow to determining if this distortion produced by pulse shaping filter could be acceptable or not. This distortion is produced under the effect of quantization error and the response of non ideal impulses. This EVM is measured of SNR in digital modulation which represents the regular orientation energy of the signal to mean square error. Finally, the HDL generated code as of the transmitter has synthesized by ISE software from Xilinx products to the Vertex 5 FPGA board with 300 MHz running rate by using specific command. The simulation and implementation results of QPSK transmitter shown the optimization of HDL code as illustrated in the status and device utilization summary which is reported by ISE software as illustrated in Table 1. This table provides the total number of LUT and Slices used in the proposed system which represent the total area used in FPGA.

TABLE 1
DEVICE UTILIZATION SUMMARY OF QPSK TRANSMITTER

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	14,436	30,720	46%	
Number of 4 input LUTs	8,322	30,720	27%	
Logic Distributaion				
Number of occupied Slices	7,326	15,360	47%	
Number of Slices containing only related logic	7,326	6,187	100%	
Number of Slices containing unrelated logic	0	6,187	0%	
Total Number of 4 Input LUTs	10,290	30,720	26%	
Number used as logic	8,733			
Number used as route-thru	210			
Number used for Dual Port RAMs	42			
Number used as Shift registers	176			
Number of bonded IOBs	93	448	20%	
Number of BUFG/BUFGCTRLs	6	32	12%	
Number used as BUFGs	6			
Number used as BUFGCTRLs	0			
Number of DSP48s	6	192	2%	
Number of RPM macros	1			
Total equivalent gate count for design	198			
Additional JTAG gate count for IOBs	6,474			

IV. CONCLUSION

The proposed HDL of QPSK modulation scheme has use a number of functional blocks to optimize the overall power compared with existing concept of this type of modulation techniques. The device utilization summary shown more area than the current design while the timing report observe high speed and throughput in suggested design of QPSK scheme. This result has expected and the gain from

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change of some components is to reduce the power consumption and utilize the LUT by about 27% with 47% in slices area. Hence, the most important is to choice algorithms allow toward lower clock rate with small bits numbers. Meaning that the clock and bits reduction will reduce the power in many algorithms is become more important in wireless communication systems. Enough methodology where demonstrated on the QPSK and HDL optimization with FPGA requirements in implementation phase. Future work need to propose the construction of transmit modulator configuration to minimize the FPGA area imagination better performance and power optimize.

REFERENCES

[1] J. Suviola, M. Allen, M. Valkama, and M. Renfors, ``Real-time FPGA implementation and measured performance of i/q modulation based frequency synthesizer,'' in *19th European Signal Processing Conference,* Catalonia, Spain, 2011.

[2] A. Milik and A. Pulka, ``Complex mathematical models simulation on mixed HDL-simulink platform,'' in *2008 Conference on Human System Interactions,* California, CA, 2008.

[3] S. N. Cubero, S. McLernon, and A. Sharpe, ``Over-speeding warning system using wireless communications for road signs and vehicles,'' *Journal of Advances in Technology and Engineering Studies*, vol. 2, no. 5, pp. 140-155, 2016. doi: https://doi.org/10.20474/jater-2.5.2

[4] Popescu, S. O., and Gontean, A. S., and Budura, G, ``Simulation and implementation of a BPSK modulator on FPGA,'' in *6th IEEE International Symposium on Applied Computational Intelligence and Informatics,* Timisoara, Romania, 2011.

[5] A. S. Gontean, S. O. Popescu, and G. Budura, ``BPSK system on spartan 3E FPGA,'' in *IEEE 10th International Symposium on Applied Machine Intelligence and Informatics,* Timisoara, Romania, 2012.

[6] K. Punaiyah and H. Singh, ``Biped robot for walking and turning motion using raspberry pi and arduino,'' *International Journal of Technology and Engineering Studies*, vol. 3, no. 2, pp. 49-58, 2017. doi: https://doi.org/10.20469/ijtes.3.40002-2

[7] O. Jingzhao and K. P. Viktor, ``MATLAB/simulink based hardware/software cosimulation for designing using FPGA configured soft processors,'' in *Proceedings of the 19th IEEE International Parallel and Distributed Processing Symposium,* New York, NY, 2005.

[8] Xilinx, ``System generator for DSP, getting started guide.'' 2008. [Online]. Available: https://urlzs.com/RLtR

[9] X. Comapny, ``Spartan 3E FPGA starter kit board. user guide,'' 2011. [Online]. Available: https://urlzs.com/yrxy

[10] S. M. M. Kahaki, W. Ismail, M. J. Nordin, N. S. Ahmad, and M. Ahmad, ``Automated age estimation based on geometric mean projection transform using orthopantomographs,'' *Journal of Advances in Technology and Engineering Studies*, vol. 3, no. 1, pp. 6-10, 2017. doi: https://doi.org/10.20474/jater-3.1.2

[11] A. Shukla and M. Deshmukh, ``Comparative study of various FFT Algorithm Implementation on FPGA 1,'' *International Journal of Emerging Trends*, vol. 1, no. 1, pp. 45-50, 2012.

[12] I. Sugiyatno, Djunaedi., and N. A. Mahardiono, ``Modelling and simulation of hybrid control system in solar cell-battery-super capacitor,'' *International Journal of Technology and Engineering Studies*, vol. 1, no. 3, pp. 74-80, 2015. doi: https://doi.org/10.20469/ijtes.40002-3

[13] S. R. Tambakhe and P. Thakare Ajay, ``Design and simulation of mathematical models-an DSP and digital communication based approach,'' *International Journal of Engineering Research and Applications*, vol. 4, no. 4, pp. 43-49, 2014.

[14] B. K. Sujatha, ``Optimization of QPSK MODEM with AWGN implemented in FPGA,'' in *2017 International Conference on Inventive Systems and Control,* Bangkok, Thiland, 2017.

[15] R. W. Stewart, L. Crockett, D. Atkinson, K. Barlee, D. Crawford, I. Chalmers, and E. Sozer, ``A low-cost desktop software defined radio design environment using MATLAB, simulink, and the RTL-SDR,'' *IEEE Communications Magazine*, vol. 53, no. 9, pp. 64-71, 2015. doi: https://doi.org/10.1109/mcom.2015.7263347

[16] E. Grayver, *Implementing Software Dened Radio*. New York, NY: Springer, 2012.

[17] L. Goeller and D. Tate, ``A technical review of software defined radios: Vision, reality, and current status,'' in *IEEE Military Communications Conference,* Baltimore, MD, 2014.

[18] M. B. Sruthi, M. Abirami, A. Manikkoth, R. Gandhiraj, and K. P. Soman, ``Low cost digital transceiver design for software defined radio using RTL-SDR,'' in *International Mutli-Conference on Automation, Computing, Communication, Control and Compressed Sensing,* Kottayam, Kerala, 2013.

ISSN: 2414-4592
DOI: 10.20474/jater-4.5.4

[19] a. A. A. Petrova, M. and P. Mahonen, ``System-oriented communications engineering curriculum: Teaching design concepts with SDR platforms,'' *IEEE Communications Magazine*, vol. 52, no. 5, pp. 202-209, 2014. doi: https://doi.org/10.1109/mcom.2014.6815913

[20] S. G. Bilen, A. M. Wyglinski, C. R. Anderson, T. Cooklev, C. Dietrich, B. , and J. H. Reed, ``Software-defined radio: A new paradigm for integrated curriculum delivery,'' *IEEE Communications Magazine*, vol. 52, no. 5, pp. 184-193, 2014. doi: https://doi.org/10.1109/mcom.2014.6815911

[21] S. B. Junior, V. C. De Oliveira, and G. B. Junior, ``Software defined radio implementation of a QPSK modulator/demodulator in an extensive hardware platform based on FPGAs Xilinx ZYNQ,'' *Journal of Computer Science*, vol. 11, no. 4, pp. 598-611, 2015. doi: https://doi.org/10.3844/jcssp.2015.598.611

[22] R. M. Ferreira, A. Shahpari, F. P. Guiomar, S. B. Amado, M. Drummond, J. D. Reis, and A. L. Teixeira, ``Hardware optimization for carrier recovery based on mth power schemes,'' in *Optical Fiber Communication Conference,* Anaheim, CA, 2016.

[23] N. J. Gaurihar, I. R. Khadse, T. S. Ghonade, A. Borkar, A. Singh, and M. M. Patil, ``Design and implementation of LDPC codes and turbo codes using FPGA,'' *International Research Journal of Engineering Technology*, vol. 3, no. 3, pp. 1683-1687, 2016.

[24] D. Kuswidiastuti, S. Suwadi, T. Suryani, and D. Elvia, ``Implementation and performance analysis of convolution codeon warp (wireless open access research platform),'' *JAVA Journal of Electrical and Electronics Engineering*, vol. 13, no. 1, pp. 56-70, 2016.

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